nCELL-T5000 & ACCELERATION CARD DATASHEET

# nCELL-T5000

## 5G Virtualized Units

5GNR

4 Cells

3GPP Release 15/R16*

DL 1.5Gbps/UL 260Mbps

400 Active Users per cell

The nCELL-T5000 from SUNWAVE is used to realize 5G NR base station processing unit to centrally control and manage the entire base station system. It realizes direct access and data interaction with 5G core network, with NGAP and XnAP interface. Also, the product realizes 5G NR access network protocol stack function, RRC, PDCP, SDAP, RLC, MAC and PHY protocol layer functions, as well as baseband processing functions.

# nCELL-T5000 & ACCELERATION CARD DATASHEET

| PROCESSOR PARAMETERS | |
|---|---|
| **CPU** | CPU Intel® Xeon® D-2177NT Processor 105W (14C/28T)<br>CPU Intel® Xeon® D-2187NT Processor 110W (16C/32T) |
| **Photolithography** | 14nm |
| **Processor Base Frequency** | XeonD-2177NT Processor – 1.9GHz<br>XeonD-2187NT Processor – 2.0GHz |
| **Maximum Turbo Frequency** | 3.00 GHz |
| **Cache** | 19 MB |
| **Memory Type** | DDR4-2666 |
| **Supported ECC Memory** | Yes |
| **Maximum Number of Memory Channels** | 4 |
| **Maximum Memory Speed** | 2667 MHz |
| **Maximum Memory (Depending on Memory Type)** | 256 GB |
| **Chipset** | Intel® Xeon® SoC |
| **Size** | 482.6 x 420 x 44.5 mm \| 19.00 x 16.54 x 1.75 in |
| **Weight** | 6.5 kg \| 14.33 lbs |
| **Power Supply** | 450W 1+1 redundant PSUs<br>100V to 240V AC @50-60Hz<br>-36V to -72V DC |
| **MTBF** | 150,000 h |

| FUNCTIONAL INDICATORS | |
|---|---|
| **Standard** | 3GPP R15/R16* |
| **Server Platform** | Xeon D-2177NT Processor<br>Xeon D-2187NT Processor |
| **Maximum Number of Cells** | 2 (XeonD-2177NT Processor)<br>4 (XeonD-2187NT Processor) |
| **Carrier Bandwidth** | 20MHz/40MHz/50MHz/60MHz/80MHz/100 MHz |
| **Subcarrier Spacing** | 30 kHz |
| **Number of Active Users** | 400 users |
| **Downlink Peak Rate** | 1.5 Gbps (DDDSU), 658Mbps (DSUUU) |
| **Uplink Peak Rate** | 260 Mbps (DDDSU), 669Mbps (DSUUU) |
| **Maximum Number of Data Streams** | Downlink 4 streams |
| | Uplink 2 streams |
| **Number of Concurrently Scheduled Users** | 4 users / Slot |

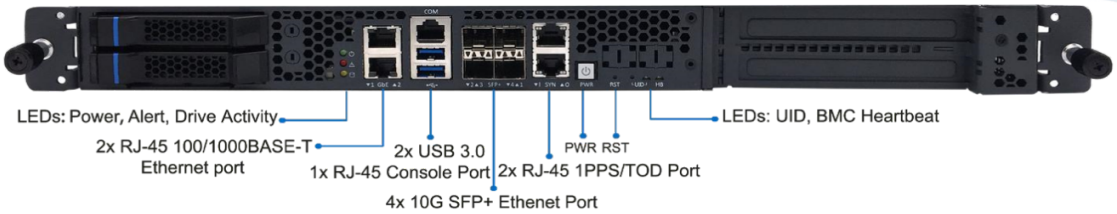
# nCELL-T5000 & ACCELERATION CARD DATASHEET

| | |
|---|---|
| **RF Front End** | RRU with FPGA/DSP |
| **RF Front End** | < 6 GHz |
| **Duplex Mode** | TDD, FDD |
| **BS Spatial Layers** | 4 |
| **UE Spatial Layers** | 2 |
| **Fronthaul Bandwidth** | 10G |
| **Number of Fronthaul Interfaces** | 4 |
| **Return Bandwidth** | 10G |
| **Number of Return Interfaces** | 2 |

Note:"*"means it is on roadmap.

| **ENVIRONMENTAL SPECIFICATIONS** | | |
|---|---|---|
| **Temperature** | **Operation** | -5 °C ~ +55 °C \| +23 °F ~ +131 °F |
| | **Storage** | -40 °C ~ +70 °C \| -40 °F ~ +158 °F |
| **Humidity** | **Operation** | 10% ~ 85% RH @40 °C, non-condensing |
| | **Storage** | 5% ~ 90% RH, non-condensing |
| **Fan** | 6 fans, adaptive speed | |
| **Shock** | Operating time: Half sine 2G, 11ms pulse, 100 pulses in each direction | |
| | Non-operating: Trapezoid, 25G, 170 inches/sec DeltaV, 3 drop tests in each direction | |
| **Vibration** | Non-operating time: 2.2Grms, 10 minutes per axis per direction | |
| **Decibel** | Sound pressure < 75 dBA @1m, all fans run at maximum speed | |

**DEVICE INTERFACE**

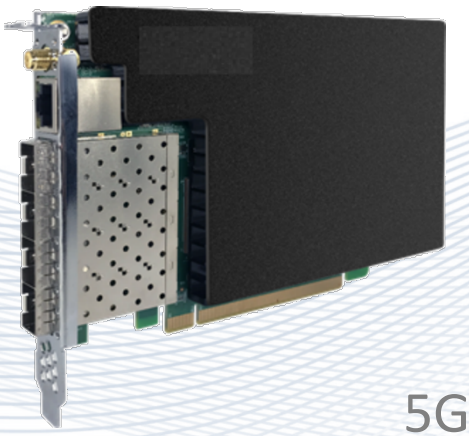



| | |
|---|---|
| **IO Interface** | 2 x RJ-45 100/ 1000BASE-T Ethernet port |
| | 4 x 10G SFP+ Ethernet port |
| | 2 x RJ-45 1PPS/ TOD port |
| | 1 x RJ-45 console port |
| | 2 x USB 3.0 |
| **Back Interface** | 1 x VGA rear |
| | 1 x Power Plug |

| INTERNAL INTERFACE | |
|---|---|
| **IO Interface** | 1 x USB 2.0 |
| | 1 x COM |
| | 4 x 1PPS SMA input/ output |
| **PCIe** | 2 x PCIe x16 Gen3 single-slot FHFL interfaces, up to 110W each |
| | Or<br>1 x PCIe x16 Gen3 single-slot FHFL interface, up to 250W<br>1 x PCIe x8 Gen3 OCP NIC v2 |
| **Storage** | 2 x 2.5” hot-swappable SATA 6 Gb/s |
| | 1 x onboard M.2 NVME socket, 2242 M Key |
| | 1 x onboard M.2 NVME socket, 2280 M Key |

# FGAF Acceleration Card

## 5G Virtualized Units



5G ORAN Prequel

5G Baseband Processing Acceleration

10G Ethernet 1588V2 Clock Synchronization Service

The integrated fronthaul accelerator card FGAF uses Xilinx's Zynq Ultra Scale+ MPSOC and Kintex Ultra Scale+ FPGA to realize the functions of baseband processing acceleration and data forwarding, and meets the application requirements of high bandwidth, low latency and multi-cell deployment required by the 5G BBU system. Very high integration and ease of use.

This card is a single-slot, full-height half-length (FHHL) card, using PCIeGen3x16 interface (supports bifurcation into two sets of Gen3x8 interfaces) to connect to the system, and externally supports 4 SFP+ optical ports.

The card is equipped with a high-precision clock source and clock phase-lock circuit, supports external 1588V2 and GPS input, and can provide stable clock synchronization services to the next-level network node through the SFP+ fronthaul interface.

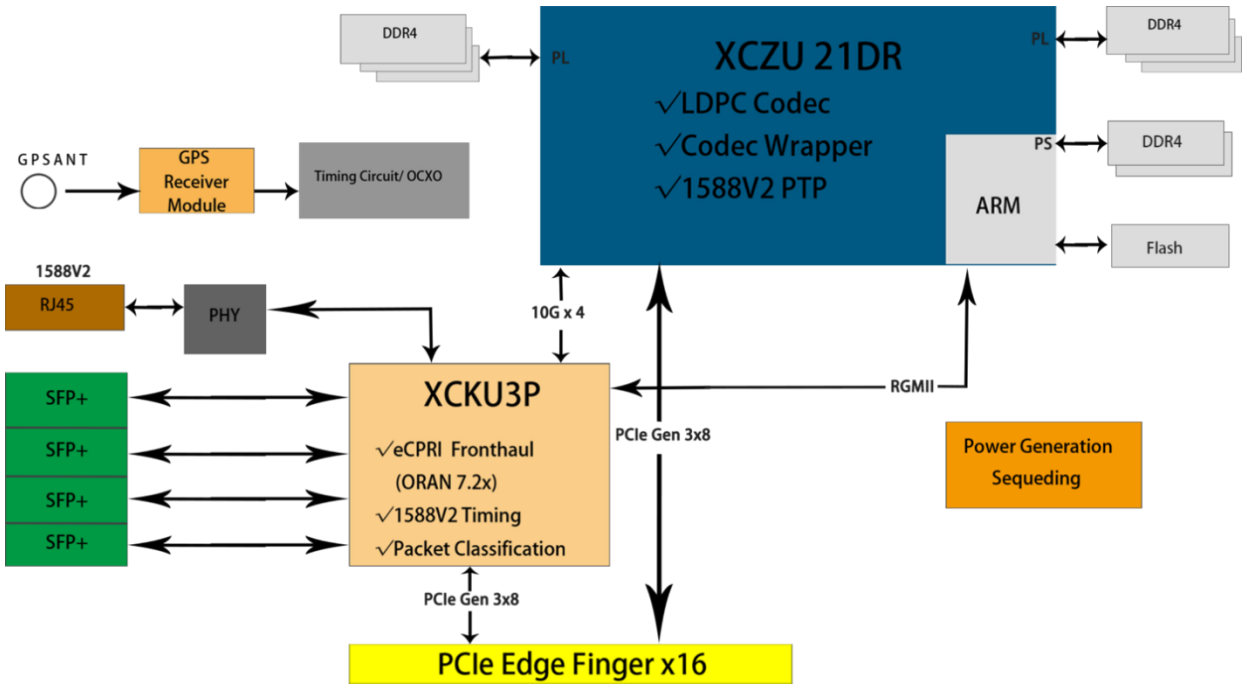
# nCELL-T5000 & ACCELERATION CARD DATASHEET

| BASEBAND PROCESSING ACCELERATION PERFORMANCE | | |
|---|---|---|
| | **Throughput Rate** | **Delay** |
| **LDPC Encoding** | 17.8 Gbps | 14μs |
| **LDPC Decoding** | 8.1 Gbps | 16μs |

| FRONTHAUL DATA FORWARDING PERFORMANCE | | | |
|---|---|---|---|
| | **Downlink Rate** | **Uplink Rate** | **Remarks** |
| **Single optical port rate** | 10 Gbps | 10 Gbps | Full package mode, 4 concurrent ports |
| **Single optical port rate** | 9 Gbps | 9 Gbps | Burst32, large and small packet interval mode, 4 concurrent ports |

| CLOCK SYNCHRONIZATION PERFORMANCE | | |
|---|---|---|
| **Support Standard** | **Index** | **Uplink Rate** |
| Grand master | Support clock synchronization of 128 nodes | Number of Slavers |
| SyncE G.8262 | All 4 interfaces support | |
| Keep ability | 1.5μs over 8 Hours | Choose high stability OCXO |

## SINGLE BOARD FRAME



# nCELL-T5000 & ACCELERATION CARD DATASHEET

| SINGLE BOARD SPECIFICATIONS | | | | |
|---|---|---|---|---|
| **Physical layer acceleration** | LDPC codec | Codec encapsulation logic, supports CRC, rate matching and de-rate matching | | |
| **Fronthaul** | 4x10G eCPRI<br>Supports 1588V2 | Data aggregation | Data cache | Package classification management |
| **Clock circuit** | Onboard OCXO, high-precision phase-locked loop synchronization circuit | Onboard GPS receiver module | Supports external 1588V2 input | |

| CHIPSET SPECIFICATIONS | | |
|---|---|---|
| **Chip Model** | Xilinx \| Zynq Ultra Scale Plus RFSoC \| XCZU21DR | |
| | Xilinx \| Kintex Ultra Scale+ \| XCKU3P | |
| **System Resource** | **XCZU21DR**<br>• System Logic cells - 930K<br>• CLB LUT - 425K<br>• SDFEC -8<br>• DSP Slices - 4,272<br>• BRAM - 38.0Mb<br>• URAM - 22.5Mb | **XCKU3P**<br>• System Logic cells - 365K<br>• CLB LUT - 163K<br>• DSP Slices - 1,368<br>• BRAM - 12.7Mb<br>• URAM - 13.5Mb<br>• GTY Transceivers - 16 |
| **Structure Size** | Full-height, half-length (FHHL)<br>x16 PCIe form factor<br>W x H x D: 169.6 x 110.6 mm x 18.6 mm \| 6.68 x 4.35 x 0.73 in | |
| **PCIe Interface** | PCIe Gen3 x16 interface bifurcated to two PCIe Gen3 x8 | |
| **Onboard RAM Resources** | • 2xBanks of 512M x 48 –PL<br>• 1xBank of 512Mx 32 –PS<br>• Total Capacity 6GB in PL<br>• Total Capacity 2GB in PS | / |
| **Onboard FLASH Resources** | 1Gb SPI FLASH NOR SLC | 256Mb SPI FLASH NOR SLC |
| **Network Interface** | 4 SFP+ optical ports | |
| **Cooling Method** | Module with cooling teeth, cooling through internal air ducts in the case | |
| **Single Board Management** | • Single board power-up sequence management and hot reset and shutdown functions<br>• Supports local software upgrade<br>• JTAG daisy-chaining design to support burning and debugging of two devices | |

| | |
|---|---|
| | • On-board RS232 debug port<br>• On-board Ethernet debug port |
| **Single Board Working Temperature** | 0 ℃ ~ +80 ℃ \| +32 °F ~ +176 °F |
| **Single Board Power Consumption** | < 35W |
| **Single Board Clock Synchronization Mode** | • Supports external GPS antenna for GPS synchronization<br>• Supports 1588V2 time information input via external Ethernet RJ45<br>• Optional high stability crystal oscillator for local clock keeping within 8 hours with time accuracy deviation less than ±1.5μs |

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